Remarks/Arguments

Claims 1-7, 9, 11, 13 and 15-17 remain in this application.

The examiner has rejected claims 1-7, 9, 11, 13 and 15-17 under 35 USC 102(e) as being anticipated by *Dervisoglu, et al.*, United States Published Patent Application 2003/0131327.

In view of the above amendments and these remarks, reconsideration of the above noted rejections and objections is respectfully requested.

Rejections under 35 USC 102(e):

Applicant respectfully traverses the rejection of **claims 1-7, 9, 11, 13 and 15-17** under 35 USC 102(e) as being anticipated by *Dervisoglu, et al.* The independent claims are **1, 2, 4 and 5**. Independent **claim 1** calls for "test signals" generated at "test points in the IC" and routing the test signals through a hierarchy of multiplexers to "output locations" to which selected portions of the test signals, themselves, are supplied. Similarly, independent **claims 2 and 4** call for passing "test signals," themselves, from "test points" through various multiplexers to "output locations." Additionally, independent **claim 5** calls for passing "test signals" through various "selecting means" to "means for outputting selected ones of the test signals," themselves. Applicant respectfully submits that *Dervisoglu, et al.* does not teach or suggest passing or routing **actual live, active test signals**, themselves, to "output locations" or "outputting means."

The feature of passing the **actual live, active test signals**, themselves, from the test points all the way to the output locations is supported in the Specification of the present application. For instance, at page 1, lines 18-19, it states "The **internal signals** are, thus, **routed to test pads**, where the **signals** can be measured by probes touching the test pads." Also, at page 1, lines 25-27, it states "it has become necessary to multiplex the **internal signals** together to select only a subset of the **internal signals** to be sent to a reasonable number of the test pads at one time. Additionally, it is the **actual internal signals** that are routed to and measured at the

output test pads (page 3, lines 3-5). The **actual test signals** are generated at the test points (page 4, lines 20-21). Selected sets of the actual test signals are passed up through the various multiplexers to the output pads (page 5, lines 1-28).

Dervisoglu, et al., on the other hand, describes capturing test data, serializing the data, and outputting the data in serial at a serial output port on an IC. (paragraph [0045]) In other words, **captured data** is created from the generated "test signals" in *Dervisoglu, et al.* at the level of the boundary-scan registers 124. It is the captured data **created from** the test signals, **not** the test signals themselves, that is transferred through the socket access ports (220, 221, 235 and 236) upward in the hierarchical structure to the chip access port (205). Therefore the **test signals** in *Dervisoglu, et al.* are **not** passed or routed to the output location or means (i.e. the chip access port), as called for in the present claims.

There is a distinct advantage to presenting **actual live, active** signals at the output locations or outputting means. Having live information is extremely useful because some test signals may experience a glitch, and the glitch can be the root cause of an error being debugged in the IC. By measuring the **actual live, active** signals at the output locations, the glitch can be detected and used to determine the cause of the error. It is **not** possible, however, to observe the actual signals at the output locations of the IC using *Dervisoglu's* method, because *Dervisoglu, et al.* produces only **captured** data, rather than the **actual signals**. *Dervisoglu, et al.*, thus, cannot detect such a glitch in any test signal.

Additionally, the output locations and/or outputting means called for in **claims 1, 2, 4 and 5** are plural, which is necessary in order to produce more than one actual live, active test signal from the IC, since the "test signals" element in these claims is also plural. *Dervisoglu, et al.*, on the other hand, discloses that the chip access port (CAP), the test access port (TAP) and the socket access ports (SAP) comply with IEEE standard 1149.1 (paragraphs [0019], [0043], [0048], [0050] and [0053]), which calls for **serializing** output data. Additionally, *Dervisoglu, et al.* states at [0057] that "Preferably, both the boundary-scan cells (or registers) 240 and the instruction

register of the chip access port 205 are loaded and unloaded using **serial access** (i.e., scan) of their contents, via the Test Data Input (TDI) signal pin and Test Data Output (TDO) signal pin, respectively." *Dervisoglu, et al.*, therefore, teaches outputting **serialized** data at a **single** output (i.e. the Test Data Output (TDO) signal pin). It is not possible to produce **plural** actual live, active test signals using only a **single** output.

Applicant respectfully submits, therefore, that independent **claims 1, 2, 4 and 5** are not anticipated by, are not obvious in view of, and are patentable over *Dervisoglu, et al.*, at least because the reference does not teach or fairly suggest passing or routing **actual test signals** to output locations or outputting means as claimed. Additionally; since **claims 7 and 15** dependent from independent claim 1, **claims 3, 9 and 16** depend from independent claim 2, **claim 11** depends from independent claim 4, and **claims 6, 13 and 17** depend from independent claim 5; these claims also are not anticipated by, are not obvious in view of, and are patentable over *Dervisoglu, et al.* at least for the same reasons.

Additionally, independent **claim 4** further states that "a portion of the test signals are **measured**" at the output locations. The device in *Dervisoglu, et al.*, however, cannot produce "measurable" test signals at its output point, since *Dervisoglu, et al.* does not output the actual test signals, but only outputs the **captured data**, as described above. There is **no measurement** that can be made once the data has already been captured. Dependent **claims 15-17** also include this "measurement" limitation. Applicant respectfully submits, therefore, that independent **claim 4** and dependent **claims 15-17** are not anticipated by, are not obvious in view of, and are patentable over *Dervisoglu, et al.*, at least because the reference does not teach or fairly suggest that the test signals passed or routed to the output locations or outputting means are **measured** as claimed. Additionally, since **claim 11** depends from independent claim 4; this claim also is not anticipated by, is not obvious from, and is patentable over *Dervisoglu, et al.* for the same reasons.

For the reasons specifically discussed above, and others, it is believed that pending claims 1-7, 9, 11, 13 and 15-17 define patentable subject matter. Reconsideration of the previous rejections as they might apply to the pending claims is therefore respectfully requested. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

October 14, 2005
Date

L. Jon Lindsay
Registration No. 36,855
ATTORNEY FOR APPLICANT

L. Jon Lindsay
1857 W. Spring Water PL
Highlands Ranch, CO 80129
Telephone: 720-344-6189
Facsimile: 928-563-4114